FAIRCHILD
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# SSP7N60B/SSS7N60B

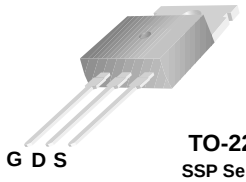
## 600V N-Channel MOSFET

### General Description

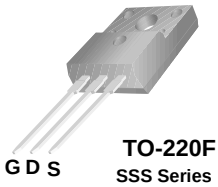
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.

### Features

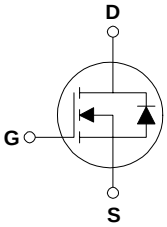
- 7.0A, 600V, $R_{DS(on)}$ = 1.2Ω @$V_{GS}$ = 10 V
- Low gate charge ( typical 38 nC)
- Low Crss ( typical 23 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- TO-220F package isolation = 4.0kV (Note 6)




**TO-220**
**SSP Series**




**TO-220F**
**SSS Series**




## Absolute Maximum Ratings

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | | SSP7N60B | SSS7N60B | Units |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 600 | | V |
| $I_D$ | Drain Current - Continuous ($T_C$ = 25°C) | | 7.0 | 7.0 * | A |
| | - Continuous ($T_C$ = 100°C) | | 4.4 | 4.4 * | A |
| $I_{DM}$ | Drain Current - Pulsed | (Note 1) | 28 | 28 * | A |
| $V_{GSS}$ | Gate-Source Voltage | | ± 30 | | V |
| $E_{AS}$ | Single Pulsed Avalanche Energy | (Note 2) | 420 | | mJ |
| $I_{AR}$ | Avalanche Current | (Note 1) | 7.0 | | A |
| $E_{AR}$ | Repetitive Avalanche Energy | (Note 1) | 14.7 | | mJ |
| dv/dt | Peak Diode Recovery dv/dt | (Note 3) | 5.5 | | V/ns |
| $P_D$ | Power Dissipation ($T_C$ = 25°C) | | 147 | 48 | W |
| | - Derate above 25°C | | 1.18 | 0.38 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | -55 to +150 | | °C |
| $T_L$ | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | | 300 | | °C |

* Drain current limited by maximum junction temperature

## Thermal Characteristics

| Symbol | Parameter | SSP7N60B | SSS7N60B | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case Max. | 0.85 | 2.6 | °C/W |
| $R_{\theta CS}$ | Thermal Resistance, Case-to-Sink Typ. | 0.5 | -- | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient Max. | 62.5 | 62.5 | °C/W |

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## Electrical Characteristics

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 600 | -- | -- | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | -- | 0.65 | -- | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 600 V, $V_{GS}$ = 0 V | -- | -- | 10 | μA |
| | | $V_{DS}$ = 480 V, $T_C$ = 125°C | -- | -- | 100 | μA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = 30 V, $V_{DS}$ = 0 V | -- | -- | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -30 V, $V_{DS}$ = 0 V | -- | -- | -100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 2.0 | -- | 4.0 | V |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 3.5 A | -- | 1.0 | 1.2 | Ω |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 40 V, $I_D$ = 3.5 A (Note 4) | -- | 8.2 | -- | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1.0 MHz | -- | 1380 | 1800 | pF |
| $C_{oss}$ | Output Capacitance | | -- | 115 | 150 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 23 | 30 | pF |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 300 V, $I_D$ = 7.0 A, $R_G$ = 25 Ω (Note 4, 5) | -- | 30 | 70 | ns |
| $t_r$ | Turn-On Rise Time | | -- | 80 | 170 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 125 | 260 | ns |
| $t_f$ | Turn-Off Fall Time | | -- | 85 | 180 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 480 V, $I_D$ = 7.0 A, $V_{GS}$ = 10 V (Note 4, 5) | -- | 38 | 50 | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 6.4 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge | | -- | 15 | -- | nC |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | -- | -- | 7.0 | A |
| $I_{SM}$ | Maximum Pulsed Drain-Source Diode Forward Current | | -- | -- | 28 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 7.0 A | -- | -- | 1.4 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_S$ = 7.0 A, $dI_F$ / dt = 100 A/μs (Note 4) | -- | 415 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 4.6 | -- | μC |

**Notes:**
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 15.7mH, $I_{AS}$ = 7.0A, $V_{DD}$ = 50V, $R_G$ = 25 Ω, Starting $T_J$ = 25°C
3. $I_{SD}$ ≤ 7.0A, di/dt ≤ 300A/μs, $V_{DD}$ ≤ $BV_{DSS,}$ Starting $T_J$ = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature
6. Only for back side in $V_{iso}$ = 4.0kV and t = 0.3s

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## Typical Characteristics

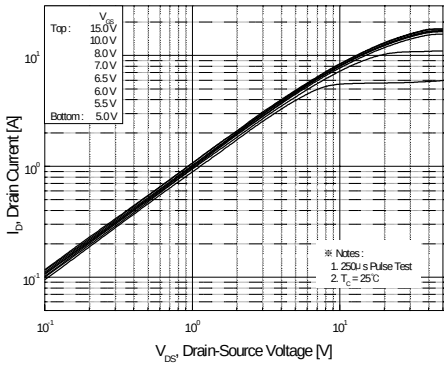


**Figure 1. On-Region Characteristics**

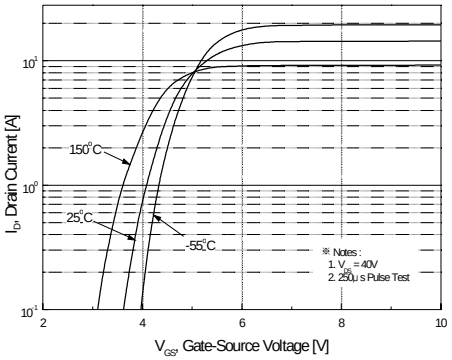


**Figure 2. Transfer Characteristics**

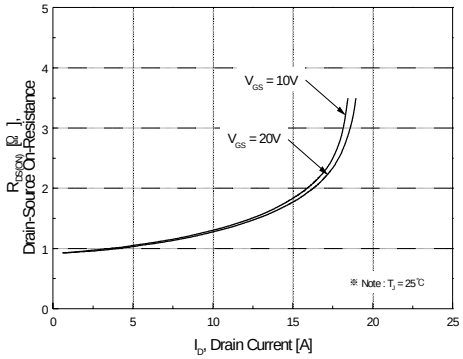


**Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage**

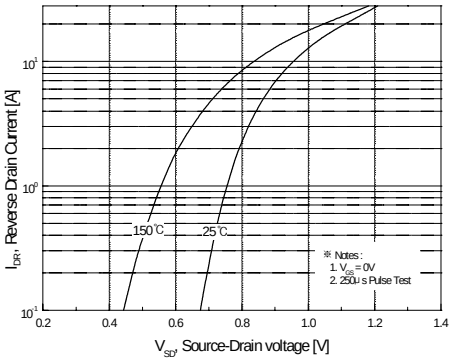


**Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature**

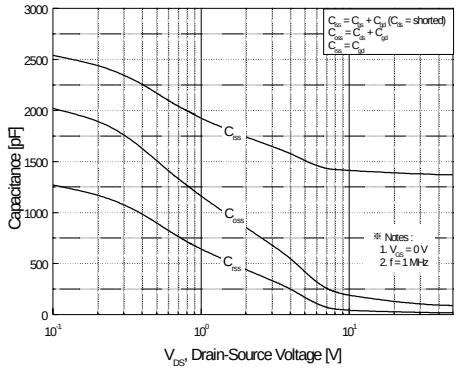


**Figure 5. Capacitance Characteristics**

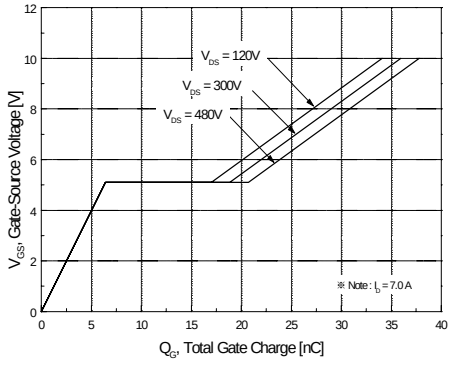


**Figure 6. Gate Charge Characteristics**

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## Typical Characteristics (Continued)

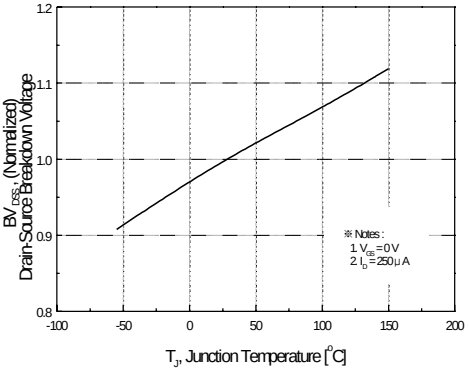


**Figure 7. Breakdown Voltage Variation vs Temperature**

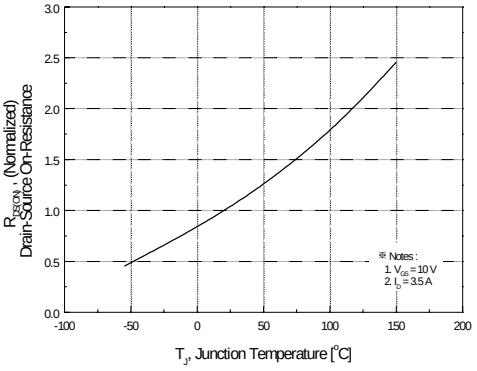


**Figure 8. On-Resistance Variation**

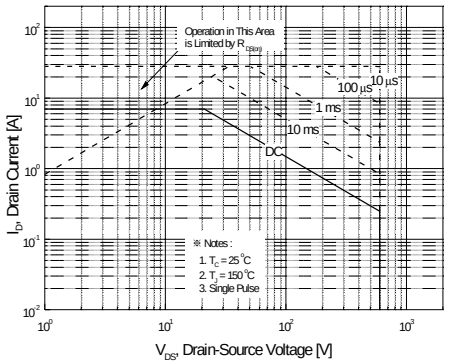


**Figure 9-1. Maximum Safe Operating Area for SSP7N60B**

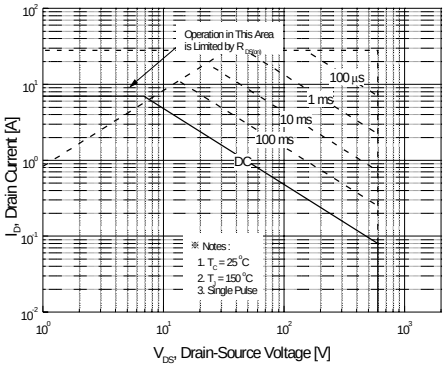


**Figure 9-2. Maximum Safe Operating Area for SSS7N60B**

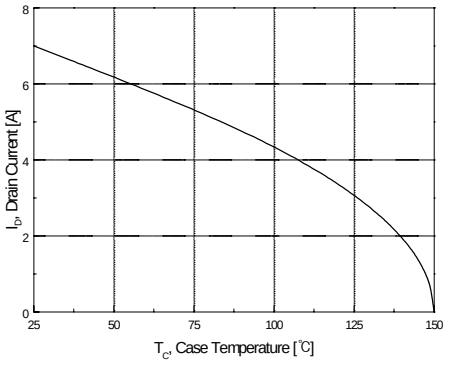


**Figure 10. Maximum Drain Current vs Case Temperature**

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## Typical Characteristics (Continued)

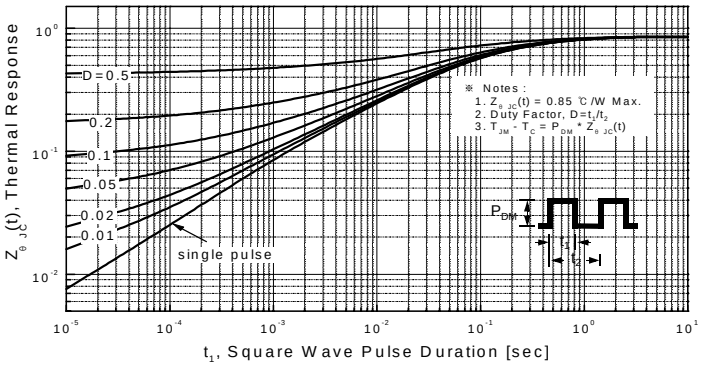


**Figure 11-1. Transient Thermal Response Curve for SSP7N60B**

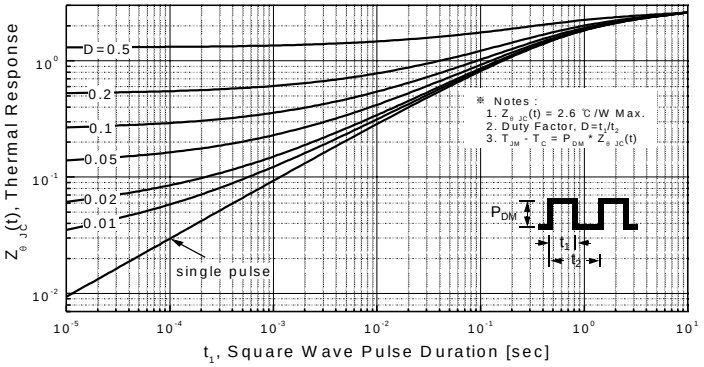


**Figure 11-2. Transient Thermal Response Curve for SSS7N60B**

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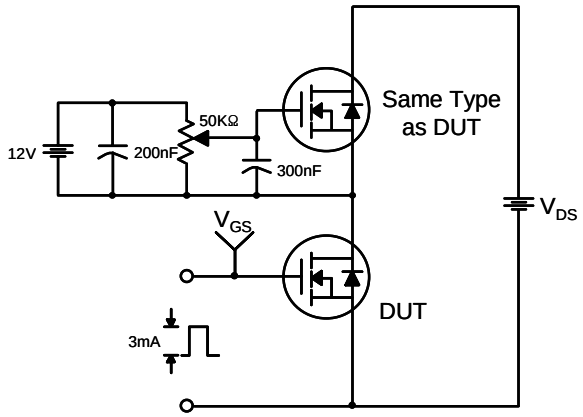
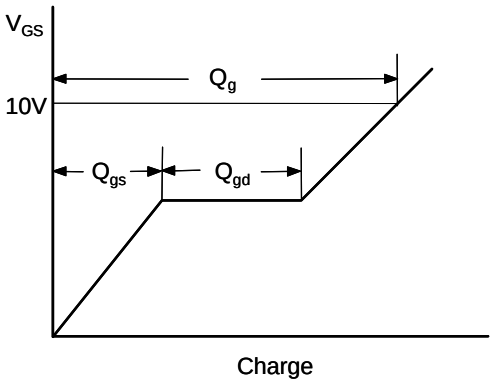
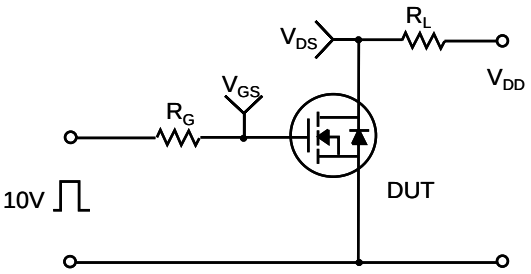
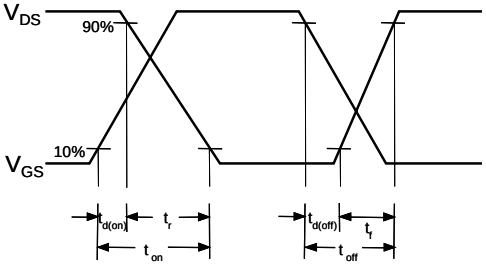
### Gate Charge Test Circuit & Waveform



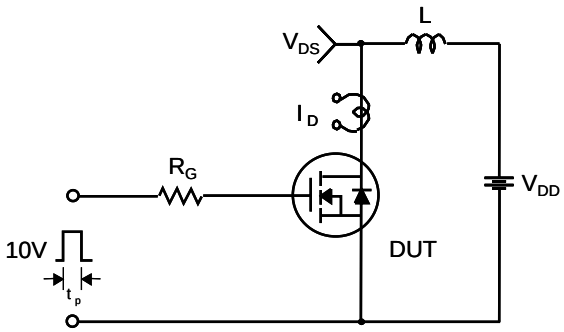




### Resistive Switching Test Circuit & Waveforms

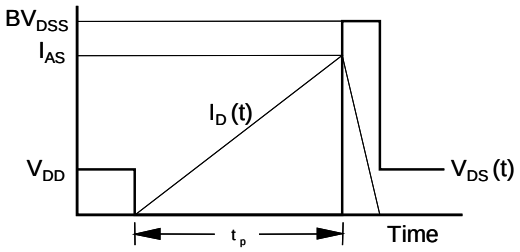



### Unclamped Inductive Switching Test Circuit & Waveforms




$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

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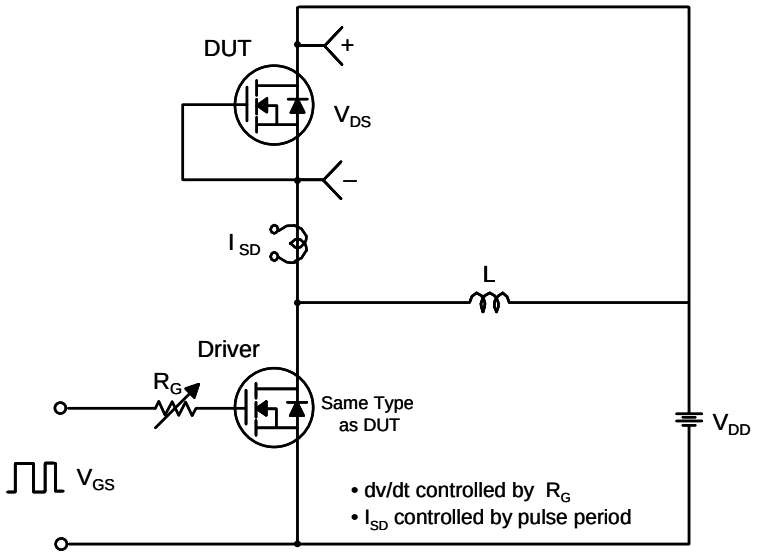
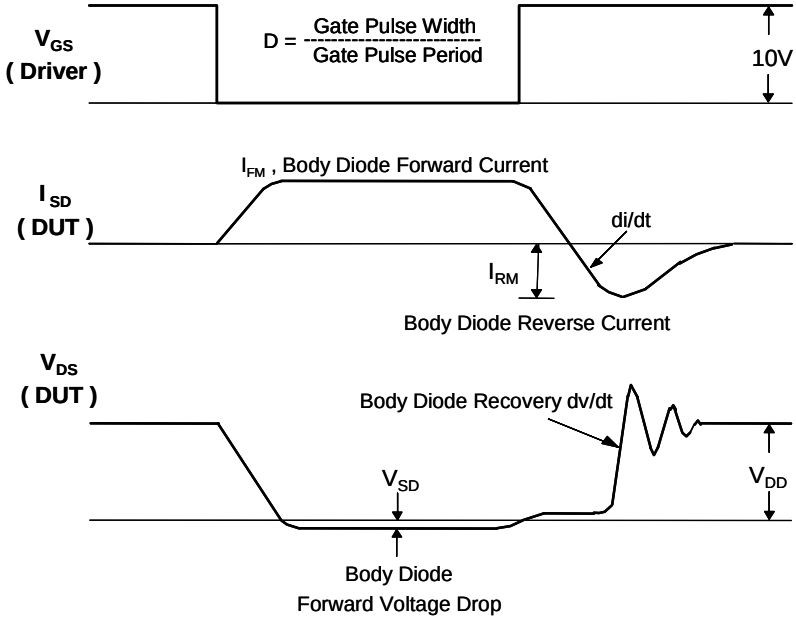
**Peak Diode Recovery dv/dt Test Circuit & Waveforms**

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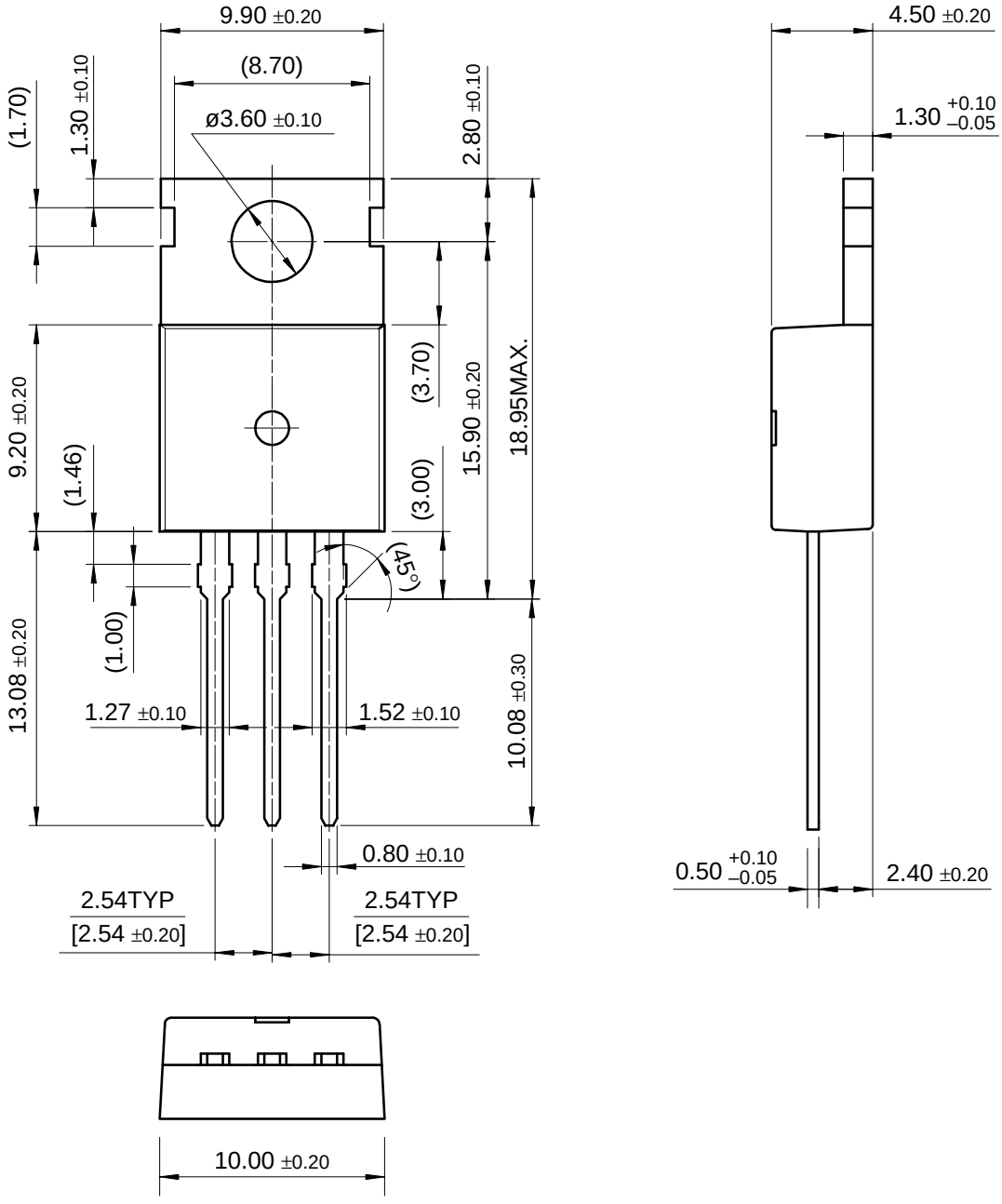
**Package Dimensions**

# TO-220




Dimensions in Millimeters

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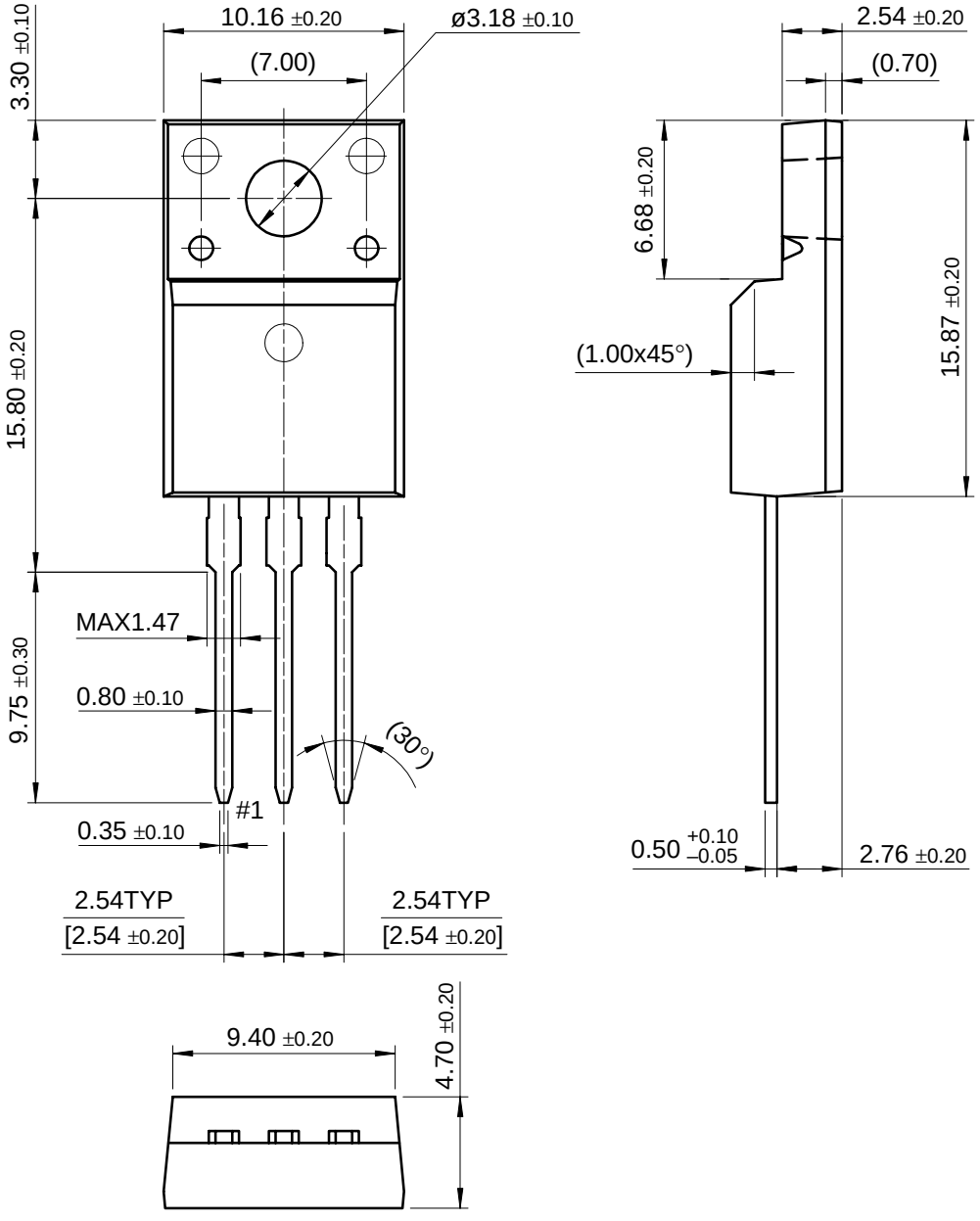
**Package Dimensions** (Continued)

# TO-220F

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| *CROSSVOLT*™ | GTO™ | POP™ | SuperSOT™-3 | |
| DOME™ | HiSeC™ | Power247™ | SuperSOT™-6 | |
| EcoSPARK™ | $I^2C$™ | PowerTrench® | SuperSOT™-8 | |
| $E^2CMOS$™ | ISOPLANAR™ | QFET™ | SyncFET™ | |
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